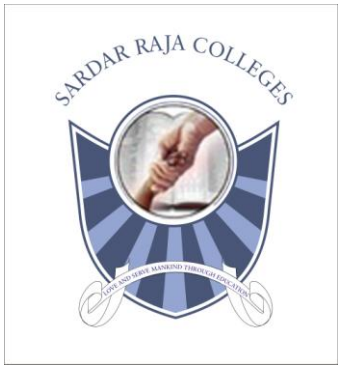
SARDAR RAJA COLLEGE OF ENGINEERING, ALANGULAM

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

MICRO LESSON PLAN



SUBJECT : DIGITAL LOGIC CIRCUITS

CODE : EE2255

CLASS : II Year / IV SEM

STAFF: Mrs. S. IDA EVANGELINE, Asst.Prof,

DEPT. OF EEE.

EE2255 DIGITAL LOGIC CIRCUITS **L T P C**
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UNIT I BOOLEAN ALGEBRA AND COMBINATIONAL CIRCUITS 9
Boolean algebra: De-Morgan's theorem, switching functions and simplification using K-maps & Quine McCluskey method, Design of adder, subtractor, comparators, code converters, encoders, decoders, multiplexers and demultiplexers.

UNIT II SYNCHRONOUS SEQUENTIAL CIRCUITS 9
Flip flops - SR, D, JK and T. Analysis of synchronous sequential circuits; design of synchronous sequential circuits – Counters, state diagram; state reduction; state assignment.

UNIT III ASYNCHRONOUS SEQUENCTIAL CIRCUIT 9
Analysis of asynchronous sequential machines, state assignment, asynchronous design problem.

UNIT IV PROGRAMMABLE LOGIC DEVICES, MEMORY AND LOGIC FAMILIES 9
Memories: ROM, PROM, EPROM, PLA, PLD, FPGA, digital logic families: TTL, ECL, CMOS.

UNIT V VHDL 9
RTL Design – combinational logic – Types – Operators – Packages – Sequential circuit – Subprograms – Test benches. (Examples: adders, counters, flipflops, FSM, Multiplexers / Demultiplexers).

L = 45 T = 15 TOTAL: 60 PERIODS

TEXT BOOKS

1. Raj Kamal, ' Digital systems-Principles and Design', Pearson education 2nd edition, 2007
2. M. Morris Mano, 'Digital Design', Pearson Education, 2006.
3. John M.Yarbrough, 'Digital Logic, Application & Design', Thomson, 2002.

REFERENCES

1. Charles H.Roth, 'Fundamentals Logic Design', Jaico Publishing, IV edition, 2002.
2. Floyd and Jain, 'Digital Fundamentals', 8th edition, Pearson Education, 2003.
3. John F.Wakerly, 'Digital Design Principles and Practice', 3rd edition, Pearson Education, 2002.
4. Tocci, "Digital Systems : Principles and applications, 8th Edition" Pearson Education.

SUBJECT DESCRIPTION AND OBJECTIVES

DESCRIPTION

Digital (electronic) circuits, represent signals by discrete bands of analog levels, rather than by a continuous range. The number of states in digital circuits is two, and they are represented by two voltage bands: one near a reference value (typically termed as "ground" or zero volts) and a value near the supply voltage, corresponding to the "false" ("0") and "true" ("1") values of the Boolean domain. Digital techniques are useful because it is easier to get an electronic device to switch into one of a number of known states than to accurately reproduce a continuous range of values.

A digital circuit is often constructed from small electronic circuits called logic gates that can be used to create combinational logic. Each logic gate represents a function of Boolean logic. A logic gate is an arrangement of electrically controlled switches, better known as transistors. Each logic symbol is represented by a different shape. The output of a logic gate is an electrical flow or voltage, that can, in turn, control more logic gates.

Logic gates often use the fewest number of transistors in order to reduce their size, power consumption and cost, and increase their reliability. Another form of digital circuit is constructed from lookup tables, (namely "programmable logic devices", though other kinds of PLDs exist).

OBJECTIVES

i. To study various number systems and to simplify the mathematical expressions using Boolean functions – simple problems.
ii. To study implementation of combinational circuits
iii. To study the design of various synchronous and asynchronous circuits.
iv. To expose the students to various memory devices.
v. To introduce digital simulation techniques for development of application oriented logic circuit.

MICRO LESSON PLAN

Hours	LECTURE TOPICS	READING
UNIT I – BOOLEAN ALGEBRA AND COMBINATIONAL CIRCUITS		
1	Boolean algebra: De-Morgan's theorem	T2
2	Switching functions	T2
3	Simplification using K-maps	T2
4	Tutorial	T2
5	Simplification using Quine McCluskey method	T2
6	Tutorial	T2
7	Design of Adder& Subtractor (AV Class)	T2
8	Design of Comparator & Code Converters	T2
9	Design of Code Converters	T2
10	Design of Encoder & Decoder	T2
11	Design of Multiplexer & Demultiplexer	T2
12	Tutorial	T2
UNIT II – SYNCHRONOUS SEQUENTIAL CIRCUITS		
13	Flip flops – SR & D	T2
14	Flip flops – JK & T	T2
15	Analysis of synchronous sequential circuits	T2
16	Design of synchronous sequential circuits	T2
17	Counters (AV Class)	T2
18	Counters	T2
19	State Diagram	T2
20	Tutorial	T2
21	State Reduction	T2
22	Tutorial	T2
23	State Assignment	T2
24	Tutorial	T2
UNIT III – ASYNCHRONOUS SEQUENTIAL CIRCUIT		
25	Analysis of Asynchronous Sequential Machines	T2
26	Analysis of Asynchronous Sequential Machines	T2
27	Tutorial	T2
28	State Assignment	T2
29	State Assignment	T2
30	Tutorial	T2
31	Asynchronous Design Problem (AV Class)	T2
32	Asynchronous Design Problem	T2
33	Asynchronous Design Problem	T2
34	Asynchronous Design Problem	T2
35	Asynchronous Design Problem	T2
36	Tutorial	T2

UNIT IV - PROGRAMMABLE LOGIC DEVICES, MEMORY AND LOGIC FAMILIES		
37	Memories: ROM,PROM & EPROM (AV Class)	T2
38	Memories: PLA	T2
39	Tutorial	T2
40	Memories: PLD,FPGA	T2
41	Tutorial	T2
42	Digital logic families: TTL	T2
43	Digital logic families: TTL	T2
44	Digital logic families: ECL	T2
45	Digital logic families: ECL	T2
46	Digital logic families: CMOS	T2
47	Digital logic families: CMOS	T2
48	Tutorial	T2
UNIT V - VHDL		
49	RTL Design – combinational logic	R1
50	Types – Operators – Packages	R1
51	Sequential circuit (AV Class)	R1
52	Subprograms	R1
53	Test benches	R1
54	Adders, Counters	R1
55	Tutorial	R1
56	Flipflops, FSM	R1
57	Tutorial	R1
58	Multiplexers	R1
59	Demultiplexers	R1
60	Tutorial	R1

Prepared by

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