EE6301 DIGITAL LOGIC CIRCUITS LT P C
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UNIT I NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES 9

Review of number systems, binary codes, error detection and correction codes (Parity and Hamming code)- **Digital Logic Families, comparison of RTL, DTL, TTL, ECL and MOS families -operation, characteristics of digital logic family.**

UNIT II COMBINATIONAL CIRCUITS 9

Combinational logic - representation of logic functions-SOP and POS forms, K-map representations minimization using K maps - simplification and implementation of combinational logic – multiplexers and demultiplexers - code converters, adders, subtractors.

UNIT III SYNCHRONOUS SEQUENTIAL CIRCUITS 9

Sequential logic- SR, JK, D and T flip flops - level triggering and edge triggering - counters - asynchronous and synchronous type - **Modulo counters -** Shift registers - design of synchronous sequential circuits – Moore and Melay models- Counters, state diagram; state reduction; state assignment.

UNIT IV ASYNCHRONOUS SEQUENTIAL CIRCUITS AND PROGRAMMABLE LOGIC DEVICES 9

Asynchronous sequential logic circuits-Transition table, flow table-race conditions, hazards &errors in digital circuits; analysis of asynchronous sequential logic circuits-introduction to **Programmable Logic Devices: PROM –PLA –PAL.**

UNIT V VHDL 9

RTL Design – combinational logic – Sequential circuit – Operators – Introduction to Packages – Subprograms – Test bench. **(Simulation /Tutorial Examples: adders, counters, flip-flops, FSM, Multiplexers /Demultiplexers).**

TOTAL (L: 45+T: 15): 60 PERIODS

TEXT BOOKS:

1. Raj Kamal, ‘ Digital systems-Principles and Design’, Pearson Education 2nd edition, 2007.

2. M. Morris Mano, ‘Digital Design with an introduction to the VHDL’, Pearson Education,2013.

3. Comer “Digital Logic & State Machine Design, Oxford, 2012.

REFERENCES:

1. Mandal ”Digital Electronics Principles & Application, McGraw Hill Edu,2013.

2. William Keitz, Digital Electronics-A Practical Approach with VHDL,Pearson,2013.

3. Floyd and Jain, ‘Digital Fundamentals’, 8th edition, Pearson Education, 2003.

4. Anand Kumar, Fundamentals of Digital Circuits,PHI,2013.

5. Charles H.Roth,Jr,Lizy Lizy Kurian John, ‘Digital System Design using VHDL, Cengage, 2013.

6. John M.Yarbrough, ‘Digital Logic, Application & Design’, Thomson, 2002.

7. Gaganpreet Kaur, VHDL Basics to Programming, Pearson, 2013.

8. Botros, HDL Programming Fundamental, VHDL& Verilog, Cengage, 2013.

SUBJECT DESCRIPTION AND OBJECTIVES

DESCRIPTION

Digital (electronic) circuits, represent signals by discrete bands of analog levels, rather than by a continuous range. The number of states in digital circuits is two, and they are represented by two voltage bands: one near a reference value (typically termed as "ground" or zero volts) and a value near the supply voltage, corresponding to the "false" ("0") and "true" ("1") values of the Boolean domain. Digital techniques are useful because it is easier to get an electronic device to switch into one of a number of known states than to accurately reproduce a continuous range of values.

A digital circuit is often constructed from small electronic circuits called logic gates that can be used to create combinational logic. Each logic gate represents a function of Boolean logic. A logic gate is an arrangement of electrically controlled switches, better known as transistors. Each logic symbol is represented by a different shape. The output of a logic gate is an electrical flow or voltage, that can, in turn, control more logic gates.

Logic gates often use the fewest number of transistors in order to reduce their size, power consumption and cost, and increase their reliability. Another form of digital circuit is constructed from lookup tables, (namely "programmable logic devices", though other kinds of PLDs exist).

OBJECTIVES:

- To study various number systems , simplify the logical expressions using Boolean functions
- To study implementation of combinational circuits
- To design various synchronous and asynchronous circuits.
- To introduce asynchronous sequential circuits and PLCs
- To introduce digital simulation for development of application oriented logic circuits.

SARDAR RAJA COLLEGE OF ENGINEERING

DEPARTMENT OF EEE

EE6301 - DIGITAL LOGIC CIRCUITS

MICRO LESSON PLAN

Weak	Hour	TITLE	TEXT & REF. BOOK
UNIT I NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES			
1st weak	1-3	Review of number systems, binary codes,	T2
	4	error detection and correction codes Parity code	T2
	5	error detection and correction codes Hamming code	T2
	6	Digital Logic Families	T2
2rd weak	7	comparison of RTL, DTL, TTL (AV CLASS)	T2
	8	comparison of ECL and MOS families	T2
	9	Operation, characteristics of digital logic family.	T2
	10-12	Problem (number systems & binary code)	T2
UNIT II COMBINATIONAL CIRCUITS			
3rd weak	1	Combinational logic circuits	T2
	2-3	representation of logic functions-SOP forms	T2
	4-5	representation of logic functions-POS forms	T2
	6	K-map representations minimization using K maps	T2
4th weak	7	simplification and implementation of combinational logic	T2
	8	multiplexers and demultiplexers(AV CLASS)	T2
	9	Code converters, adders, subtractors.	T2
	10-12	Problem (k Map, SOP & POS)	T2
UNIT III SYNCHRONOUS SEQUENTIAL CIRCUITS			
5th weak	1-2	Sequential logic- SR, JK, D and T flip flops -	T2
	3	level triggering and edge triggering counters	T2
	4-5	asynchronous and synchronous type Modulo counters	T2

	6	Shift registers(AV CLASS)	T2
6th weak	7	design of synchronous sequential circuits	T2
	8	Moore and Malay models- Counters	T2
	9	state diagram; state reduction; state assignment	T2
	10-12	Problem	T2
UNIT IV ASYNCHRONOUS SEQUENTIAL CIRCUITS AND PROGRAMMABLE LOGIC DEVICES			
7th weak	1	Asynchronous sequential logic circuits,	T2
	2-3	Transition table, flow table-Race conditions, hazards &errors in digital circuits	T2
	4-6	analysis of asynchronous sequential logic circuits	T2
8th weak	7-9	Introduction to Programmable Logic Devices: PROM –PLA – PAL (AV CLASS)	T2
	10-12	Problem	T2
UNIT V VHDL			
9th weak	1	RTL Design – combinational logic	T2
	2	Sequential circuit – Operators	T2
	3	Introduction to Packages – Subprograms – Test bench	T2
	4-6	Simulation /Tutorial Examples: adders, counters,	T2
10th weak	7-8	flip-flops, FSM (AV CLASS)	T2
	9	Multiplexers /Demultiplexers	T2
	10-12	Problem	T2

PREPARED BY

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